CLAIMS

What is claimed is:

1. A radio receiver formed as an monolithic integrated circuit containing circuitry comprising:

a bias signal generator for generating a bias signal for controlling characteristics of various components within said receiver; and

a reference oscillator that generates a stable reference frequency irrespective of temperature and process variations,

wherein said reference frequency generated by said reference oscillator is used by said bias signal generator to output a bias signal having a value that compensates for said temperature and process variations.

2. The circuitry of Claim 1 further comprising:

a local oscillator;

a mixer receiving an output frequency of said local oscillator;

an intermediate frequency amplifier receiving an output of said mixer; and

an intermediate frequency filter receiving an output of said intermediate frequency amplifier,

wherein said bias signal generator biases said local oscillator, said intermediate frequency amplifier, and said intermediate frequency filter so that characteristics of said local oscillator, said intermediate frequency amplifier, and said intermediate frequency filter are substantially independent of said temperature and process variations.

3. The circuitry of Claim 2 further comprising an automatic gain control circuit that receives a signal related to a magnitude of an intermediate frequency signal and adjusts a gain of said intermediate frequency amplifier based on said magnitude.

4. The circuitry of Claim 1 wherein in said bias signal generator comprises:

a phase-locked loop that generates a bias signal value related to a frequency of said phase-locked loop, said bias signal value being that required to yield frequency lock of said phase-locked loop with an output frequency of said reference oscillator, wherein said bias signal value compensates for said temperature and process variations.

5. A radio receiver formed as a monolithic integrated circuit comprising:

a superheterodyne receiver having an input coupled to an antenna input of said integrated circuit and providing a modulated output; and

a demodulator receiving said modulated output and outputting a digital data signal at a data output terminal of said integrated circuit,

said superheterodyne receiver and said demodulator being formed entirely on a signal monolithic integrated circuit chip.

6. The receiver of Claim 5 further comprising a digital decoder.

7. The receiver of Claim 6 wherein said decoder decodes a received encoded signal using a changing code scheme.